Claims

What is claimed is:

[c1] A method for creating a wire load model, comprising:

creating an interconnect configuration;

running a field solver to generate parasitic information for the interconnect configuration;

storing the parasitic information in an accessible format; and

running a curve-fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information.

[c2] The method of claim 1, wherein a range of widths and spacings for the interconnect configuration are chosen so that widths and spacings are larger than a minimum width and spacing specification for the interconnect configuration.

[c3] The method of claim 1, wherein the accessible format is a look-up table for the range.

[c4] The method of claim 1, wherein the curve-fitting engine is a non-linear curve-fitting engine.

[c5] The method of claim 1, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

[c6] A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for creating a wire load model, the method comprising:

creating a wire structure;

running a field solver to generate parasitic information for the wire structure;

storing the parasitic information in an accessible format; and

running a curve-fitting engine to create the wire load model, wherein running the curve-fitting engine is dependent on the parasitic information.

[c7] The method of claim 6, wherein a width and a spacing for the wire structure is chosen so that the width and spacing is larger than a minimum width and spacing specification for the wire structure.

[c8] The method of claim 6, wherein the accessible format is a look-up table.

[c9] The method of claim 6, wherein the curve-fitting engine is a non-linear curve-fitting engine with an error control mechanism.

[c10] The method of claim 6, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

[c11] A computer system, comprising:

a memory for storing a model of a circuit;

a processor for creating a wire load model, wherein the processor establishes an interconnect configuration for the circuit;

a field solver for determining parasitic information for the interconnect configuration; and

a curve-fitting engine that uses the parasitic information to generate the wire load model.

[c12] The method of claim 11, wherein a width and a spacing for the interconnect configuration is chosen so that the width and spacing is larger than a minimum

width and spacing specification for the interconnect configuration.

[c13] The method of claim 11, wherein the curve-fitting engine is a non-linear curve-fitting engine.

[c14] The method of claim 11, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

[c15] A method for creating a wire load model, comprising:

creating an interconnect configuration;

generating parasitic information for the interconnect configuration;

storing the parasitic information in an accessible format; and

creating the wire load model dependent on the parasitic information.

[c16] The method of claim 15, wherein generating parasitic information uses a field solver.

[c17] The method of claim 15, wherein creating the wire load model uses a non-linear curve-fitting engine.

[c18] The method of claim 15, wherein the parasitic information comprises at least one selected from the group consisting of an area capacitance, a coupling capacitance, and a fringe capacitance.

[c19] A wire load model creation tool, comprising:

means for creating an interconnection configuration for a structure;

means for field solving the interconnect configuration to determine parasitic information;

means for storing the parasitic information;

curve-fitting means for curve-fitting the parasitic information and using

interconnect configuration parameters to create a wire load model; and

means for controlling error in the curve-fitting means.